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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,587	01/15/2004	Boris Zabarski	060707-1180	4907
24504 7590 06/11/2007 THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 100 GALLERIA PARKWAY, NW STE 1750 ATLANTA, GA 30339-5948			EXAMINER DO, CHAT C	
			ART UNIT 2193	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/757,587

Applicant(s)

ZABARSKI ET AL.

Examiner

Chat C. Do

Art Unit

2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04/03/07; 09/27/06; 08/24/05; 01/05/04.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6, 13-25 and 32-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 13-25 and 32-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01/15/2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 08/24/05
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

1. This communication is responsive to Election/Restriction filed 04/03/2007.
2. Claims 1-6, 13-25, and 32-38 are pending in this application. Claims 1, 13, 17, 20, 32, and 36 are independent claims. In Election/Restriction, claims 7-12 and 26-31 are cancelled. This Office Action is made non-final.

Election/Restrictions

3. Applicant's election without traverse of Group I claims 1-6, 13-25, and 32-38 in the reply filed on 04/03/2007 is acknowledged.
4. The applicant comments in page 10 for claims in response to election/restriction requirement that the examiner acknowledges that any prior art used to reject the elected group will not be used to reject claims of other groups in any ensuing divisional application.

The examiner respectfully submits that the examiner did not acknowledge that any prior art used to reject the elected group will not be used to reject claims of other groups in any ensuing divisional application, but rather the exact embodiment with definite structure used to reject the elected group will not be used to reject claims of other groups in any ensuing divisional application.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

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Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-6, 13-25, and 32-38 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-6, 13-25, and 32-38 cite a method for determining a minimum/maximum value among values in accordance with a mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 1-6, 13-25, and 32-38 merely disclose steps/components for determining minimum/maximum value without further disclosing a practical/physical application or a useful and tangible result. The claims are just pre-emptive every practical application. Therefore, claims 1-6, 13-25, and 32-38 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-6, 13-15, 20-25, and 32-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Okumura et al. (U.S. 5,726,923).

Re claim 1, Okumura et al. disclose in Figures 1-9 a processor (e.g. architecture is seen in Figure 1) for determining a minimum value of a plurality of values stored in source registers (e.g. data field 11a in Figure 2 is stored the minimum value from either

source registers 6 or 11 in Figure 1) and determining an index value of a source register having the minimum value (e.g. index field 11b in Figure 2), the processor comprising: a destination register (e.g. specific register 11 in Figure 1); a first source register storing a first value (e.g. register 11 in Figure 1); a second source register storing a second value (e.g. registers 5-6 in Figure 1); means for comparing the first value stored in the first source register with the second value stored in the second source register (e.g. arithmetic logic unit 4 in Figure 1 as comparison unit as cited in col. 4 lines 28-40); means for storing the first value in the destination register when the first value is less than or equal to the second value (e.g. path of specific register 11 less than register 5 in Figure 3); and means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register (e.g. step S9 in Figure 3 which is done by index linking circuit 10 in Figure 1) when the second value is less than the first value (e.g. path goes through S9 in Figure 3).

Re claim 2, Okumura et al. further disclose in Figures 1-9 the means for comparing, the means for storing and the means for concatenating are adapted to execute sequentially within one processor cycle (e.g. col. 4 lines 45-50 and col. 5 lines 65-68).

Re claim 3, Okumura et al. further disclose in Figures 1-9 the first source register and the destination register comprise a same register (e.g. specific register 11 in Figure 1).

Re claim 4, Okumura et al. further disclose in Figures 1-9 the second source register and the destination register comprise a same register (e.g. reversed the register 11 in Figure 1).

Re claim 5, Okumura et al. further disclose in Figures 1-9 the first value is stored in N low-order bits of the first source register and the second value is stored in N low-order bits of the second register, N being an integer value (e.g. wherein N is the size of registers 5-6 and 11 for storing the data values in Figure 1).

Re claim 6, Okumura et al. further disclose in Figures 1-9 the first source register and the second source register each include an active status bit to indicate a status of the respective register, and wherein a value of a register having an active status is less than a value of a register having an inactive status (e.g. Figure 1 with the index field wherein the index field is either exist or non-exist with the data value to indicate the minimum value within values).

Re claim 13, Okumura et al. disclose in Figures 1-9 a method for determining a minimum value and a corresponding index value of a plurality of source registers of a processor (e.g. abstract and general architecture is seen in Figure 1), the method comprising the steps of: for each of the plurality of source registers (e.g. registers in memory 1, register 5, and specific registers 11x in Figure 4), comparing a value stored in the source register with a value stored in a destination register (e.g. col. 6 lines 1-20); concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the source register is less than the value stored in the destination register (e.g. step S9 in Figure 3); and wherein the destination register initially includes an index value and a value of a first source register of the plurality of source registers (e.g. Figure 2 as general data structure of each specific registers 11x in Figure 4).

Re claim 14, Okumura et al. further disclose in Figures 1-9 the steps of comparing, concatenating, and storing are implemented by a single processor instruction (e.g. col. 4 lines 45-50 and col. 5 lines 65-68).

Re claim 15, it has similar limitations cited in claim 2. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 20, Okumura et al. disclose in Figures 1-9 a processor for determining a maximum value of a plurality of values stored in source registers (e.g. col. 5 lines 38-42) and determining an index value of a source register having the maximum value (e.g. index field in Figure 2), the processor comprising: a destination register (e.g. specific register 11 in Figure 1); a first source register storing a first value (e.g. register 11 in Figure 1); a second source register storing a second value (e.g. registers 5-6 in Figure 1); means for comparing the first value stored in the first source register with the second value stored in the second source register (e.g. done by the arithmetic logic unit 4 in Figure 1); means for storing the first value in the destination register when the first value is greater than or equal to the second value (e.g. path loop in Figure 3); and means for concatenating the index value with the second value into a concatenated value (e.g. path of S9 in Figure 3) and storing the concatenated value in the destination register when the second value is greater than the first value (e.g. col. 5 lines 38-50).

Re claim 21, it has similar limitations cited in claim 2. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 22, it has similar limitations cited in claim 3. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 23, it has similar limitations cited in claim 4. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 24, it has similar limitations cited in claim 5. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 25, it has similar limitations cited in claim 6. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 32, it has similar limitations cited in claim 13 and further Okumura et al. disclose in Figures 1-9 the same architecture can be used/implemented to perform maximum detection in same manner as minimum detection (e.g. col. 5 lines 38-51). Thus, claim 32 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 33, it has similar limitations cited in claim 14. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 14.

Re claim 34, it has similar limitations cited in claim 15. Thus, claim 34 is also rejected under the same rationale as cited in the rejection of rejected claim 15.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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10. Claims 16-19 and 35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. (U.S. 5,726,923) in view of the admitted prior art.

Re claim 16, Okumura et al. fail to disclose in Figures 1-9 each of the plurality of values represents a due timestamp of a corresponding input queue for implementing Weighted Fair Queuing. However, the admitted prior art discloses each of the plurality of values represents a due timestamp of a corresponding input queue for implementing Weighted Fair Queuing (e.g. page 2 lines 1-26). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add each of the plurality of values represents a due timestamp of a corresponding input queue for implementing Weighted Fair Queuing as seen in the admitted prior art into the Okumura et al.'s invention because it would enable to process the data in prioritization for used in network processor (e.g. page 2 lines 1-5 and lines 14-18).

Re claim 17, Okumura et al. disclose in Figures 1-9 a customer premise equipment (e.g. Figure 1 as general architecture) comprising: and a processor operably connected to the interfaces and being adapted to (e.g. for getting data into memory 1 in Figure 1): compare (e.g. by arithmetic logic unit 4 in Figure 1) a first value stored in a first source register of the processor (e.g. specific register 11 in Figure 1) with a second value stored in a second source register of the processor (e.g. registers 5-6 in Figure 1); store the first value in a first destination register of the processor when the first value is less than or equal to the second value (e.g. path when the specific register 11 is less than register 5 in Figure 3); and store the second value in the first destination register of the processor (e.g. value in register 6 in Figure 1) and an index value in a second destination

register of the processor (e.g. corresponding index value of register 6 in Figure 1) when the second value is less than the first value (e.g. step S9 in Figure 3), the index value representing the second source register (e.g. Figure 2). Okumura et al. fail to disclose a network interface operably connected to a first network segment and a network interface operably connected to a second network segment. However, the admitted prior art disclose the general architecture of processor operation in network (e.g. pages 1-2) in which a network interface operably connected to a first network segment a network interface operably connected to a second network segment are standard and well-known. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the a network interface operably connected to a first network segment and a network interface operably connected to a second network segment as seen logically in the admitted prior art into Okumura et al.'s invention because it would enable to process data over the network (e.g. page 2 lines 1-26).

Re claim 18, it has similar limitations cited in claim 2. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 19, it has similar limitations cited in claim 16. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Re claim 35, it has similar limitations cited in claim 16. Thus, claim 35 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Re claim 36, Re claim 32, it has similar limitations cited in claim 17 and further Okumura et al. disclose in Figures 1-9 the same architecture can be used/implemented to perform maximum detection in same manner as minimum detection (e.g. col. 5 lines 38-

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51). Thus, claim 36 is also rejected under the same rationale as cited in the rejection of rejected claim 17.

Re claim 37, it has similar limitations cited in claim 18. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 18.

Re claim 38, it has similar limitations cited in claim 19. Thus, claim 38 is also rejected under the same rationale as cited in the rejection of rejected claim 19.

Response to Arguments

11. Applicant's arguments with respect to claims 1-6, 13-25, and 32-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. U.S. Patent No. 5,051,939 to Nakamura discloses a vector data retrieval apparatus.
- b. U.S. Patent No. 6,724,721 to Cheriton discloses an approximated per-flow rate limiting.
- c. U.S. Patent No. 6,829,217 to Bechtolsheim et al. disclose a per-flow dynamic buffer management.

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- d. U.S. Patent No. 6,397,240 to Fernando et al. disclose a programmable accelerator for a programmable processor system.
- e. U.S. Patent No. 5,894,426 to Ju discloses a maximum/minimum value determination apparatus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

June 5, 2007

